



FIG 2

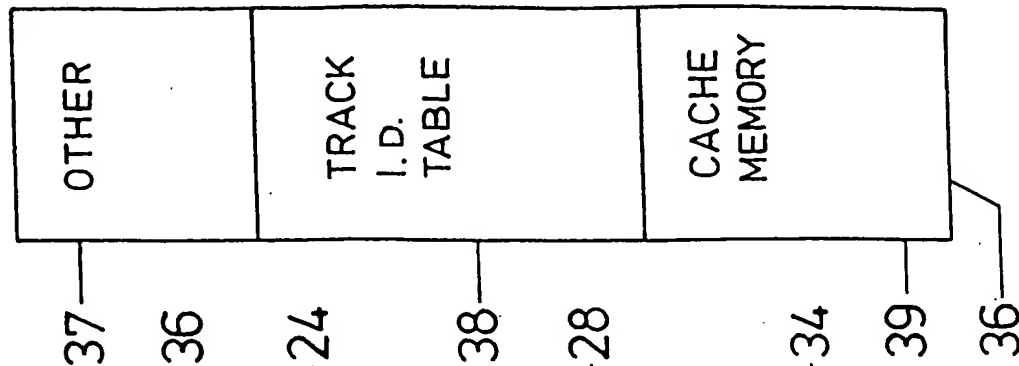


FIG 1

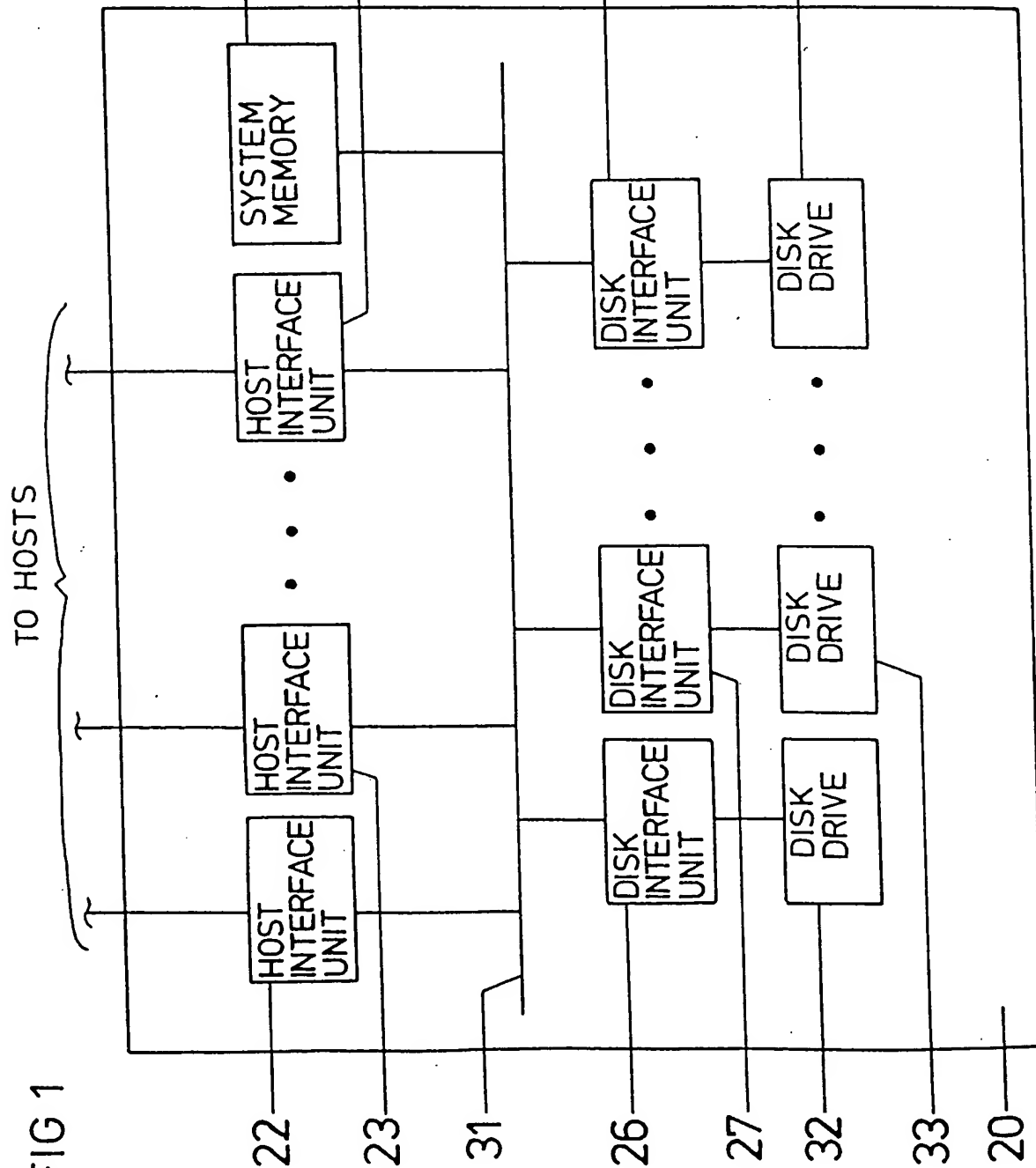


FIG 3

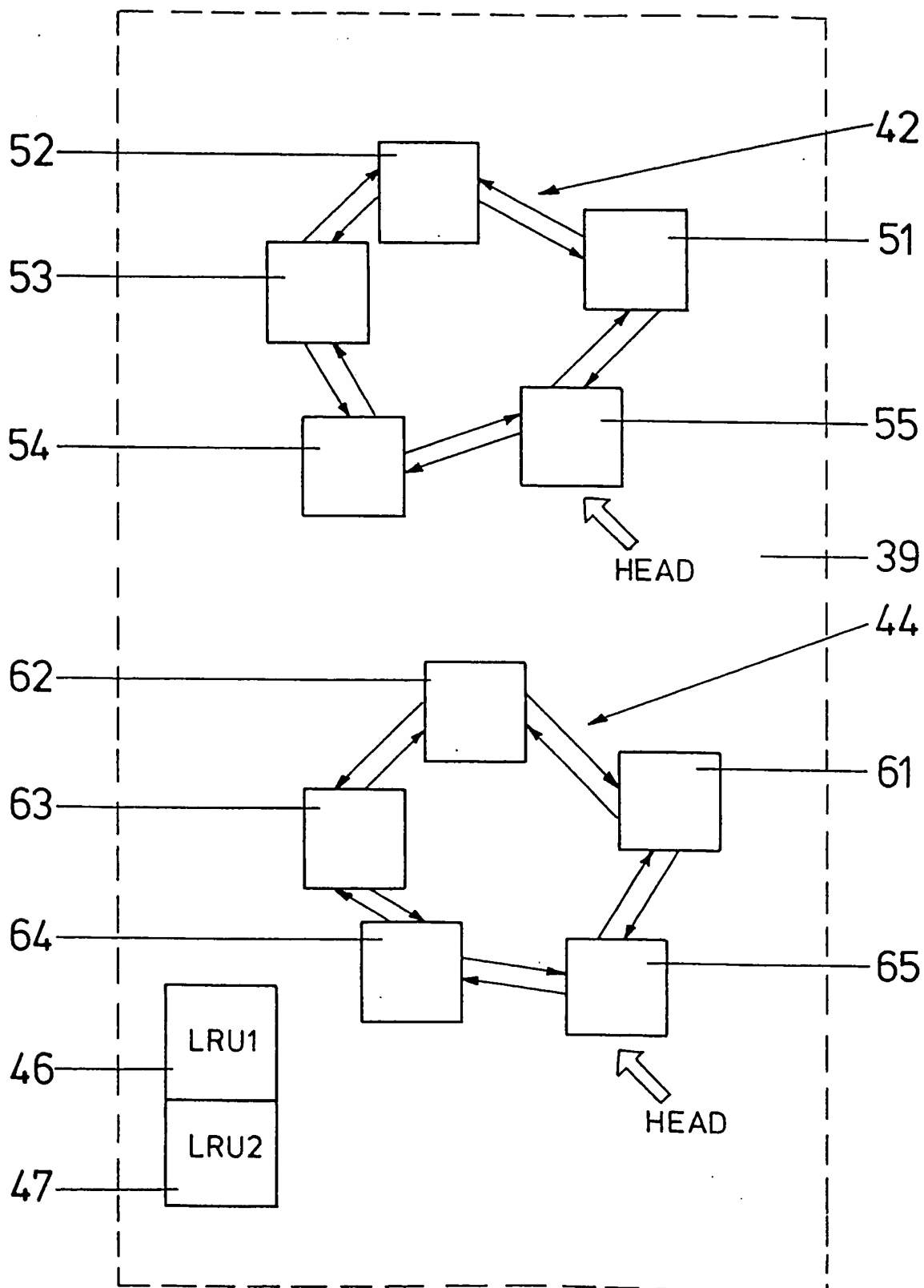
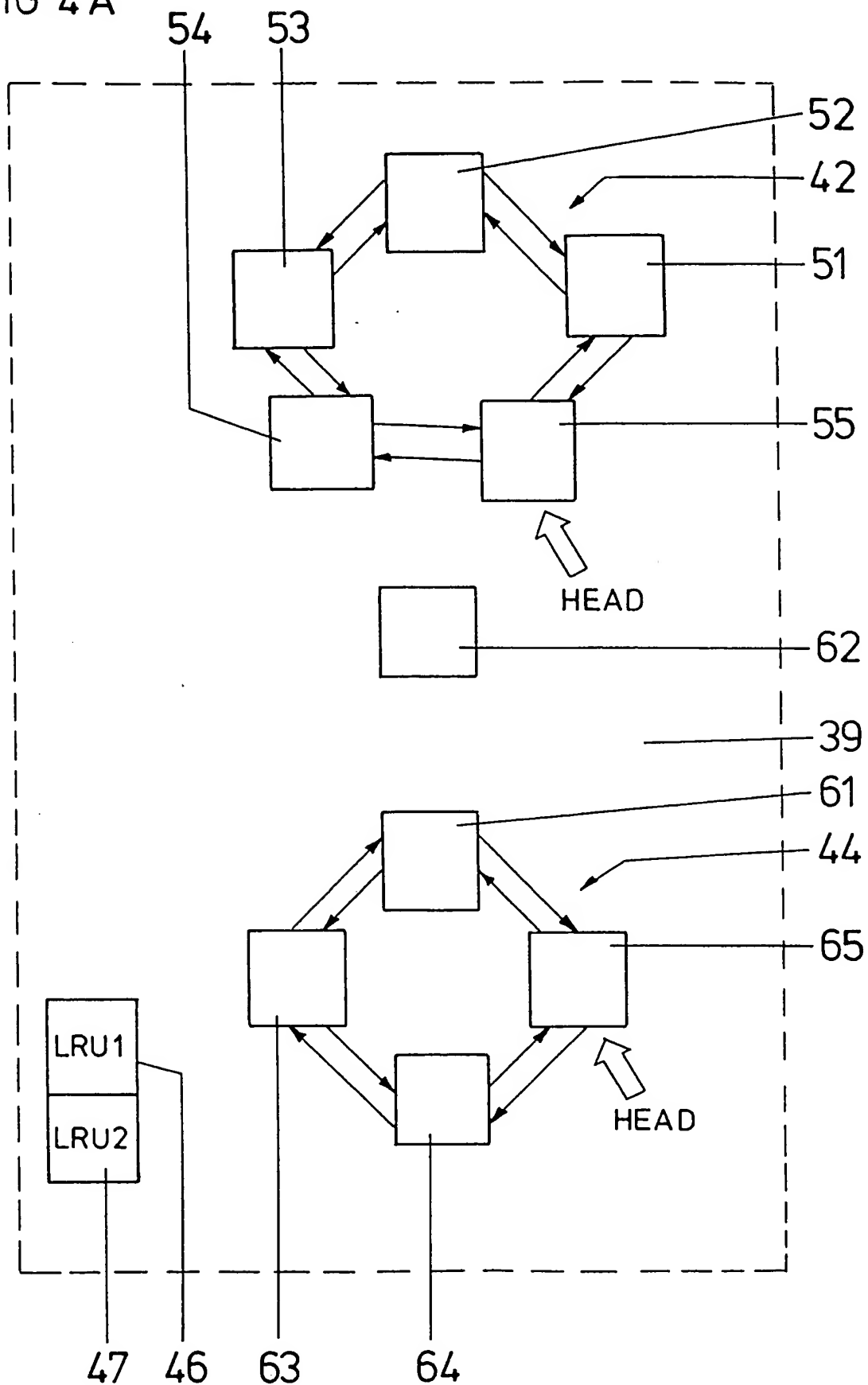


FIG 4A



The diagram illustrates a dual-channel cache system. It features two LRU (Least Recently Used) stacks, labeled 46 (LRU1) and 47 (LRU2), which manage the replacement of cache entries. These stacks are connected to two separate circular cache structures, 42 and 44, each containing four cache slots. The top cache structure 42 is associated with address lines 53, 54, 55, and 62, and has a 'HEAD' pointer. The bottom cache structure 44 is associated with address lines 61, 63, 64, and 65, and also has a 'HEAD' pointer. A central address line 39 is shown between the two cache structures. Bidirectional arrows indicate the flow of data between the LRU stacks and the cache slots, and between adjacent slots within each circular structure.

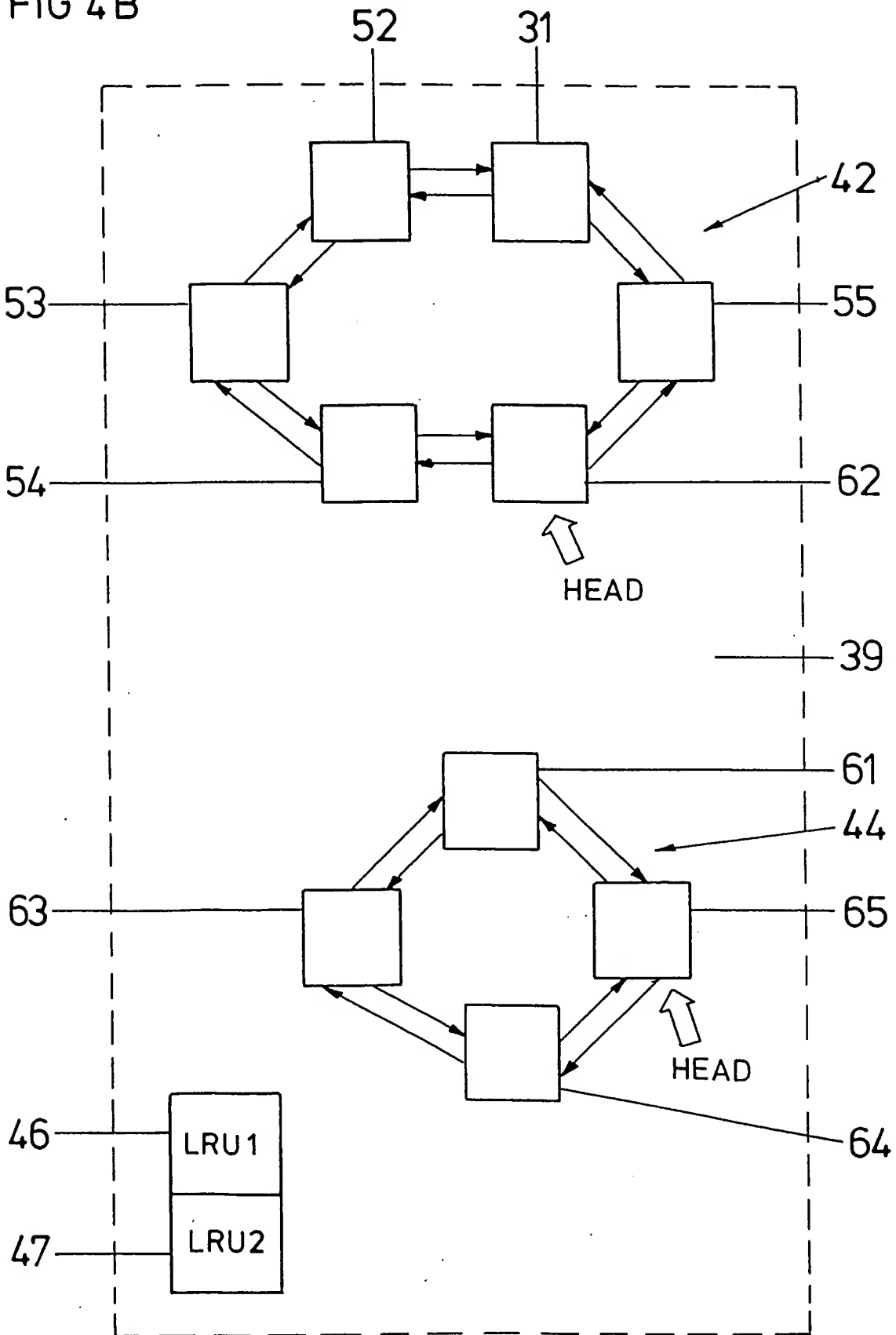


FIG 5

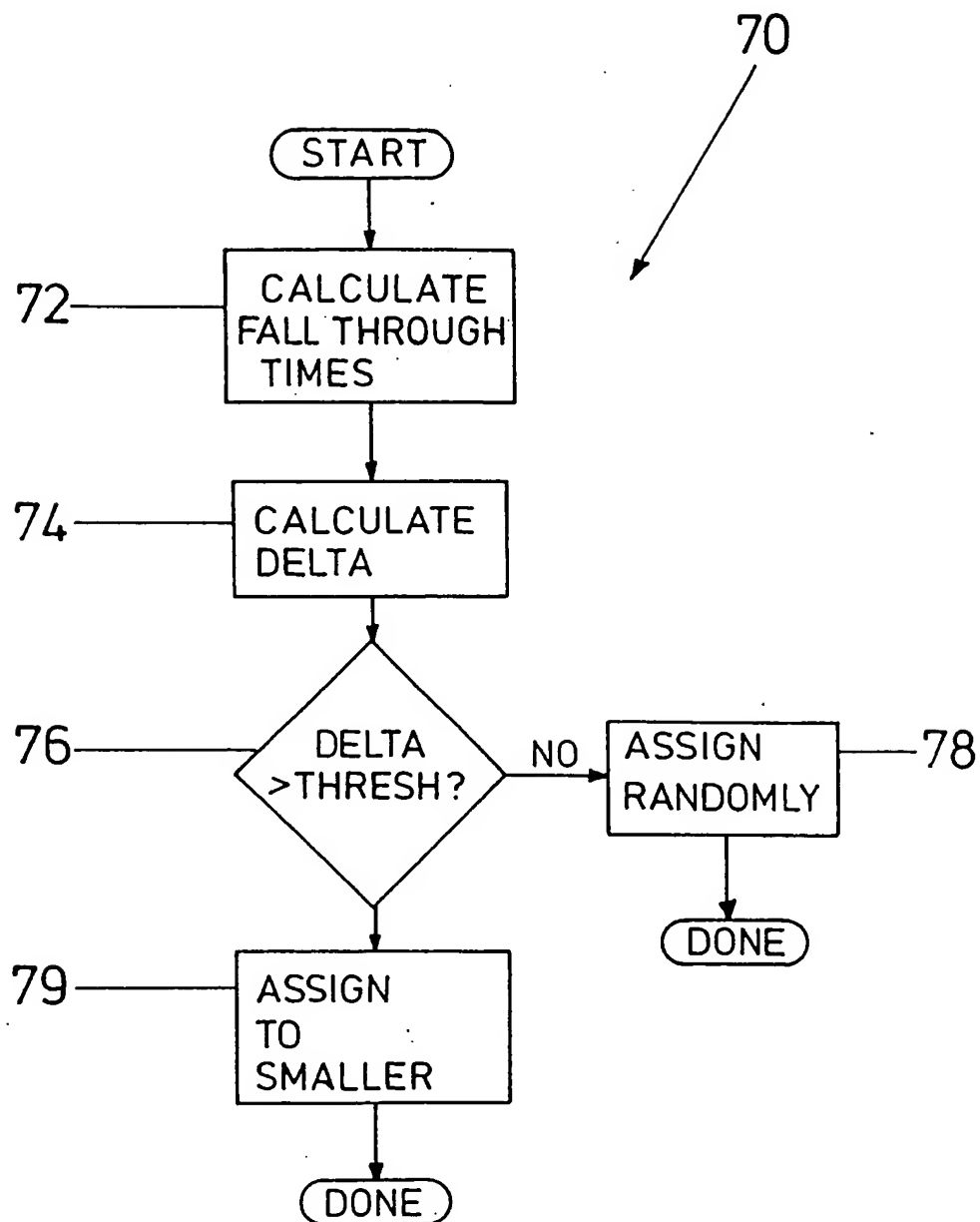


FIG 6

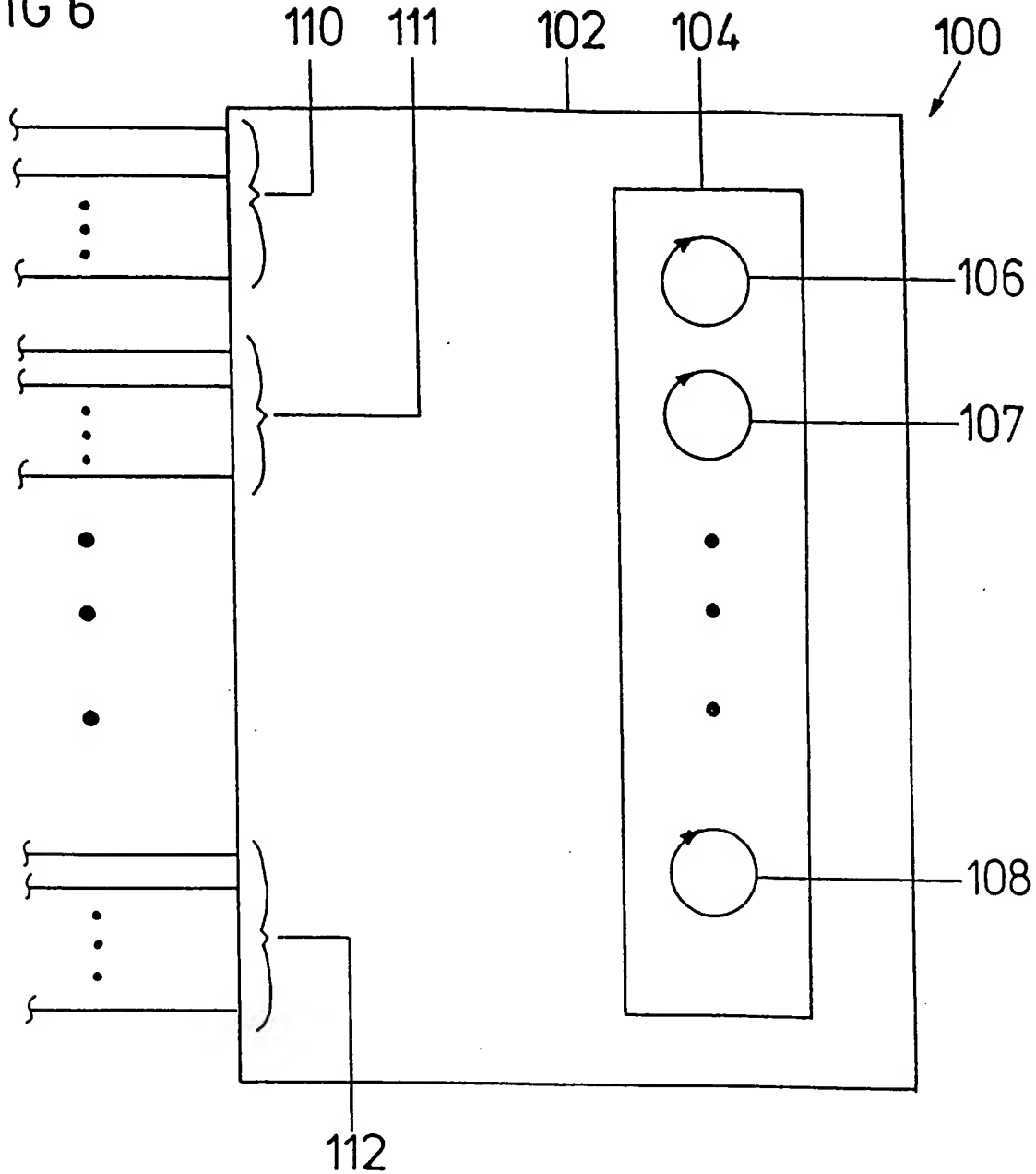


FIG 7

GROUP	LRU Mask
1	11100000
2	00011000
3	00000110
4	00000001

FIG 8

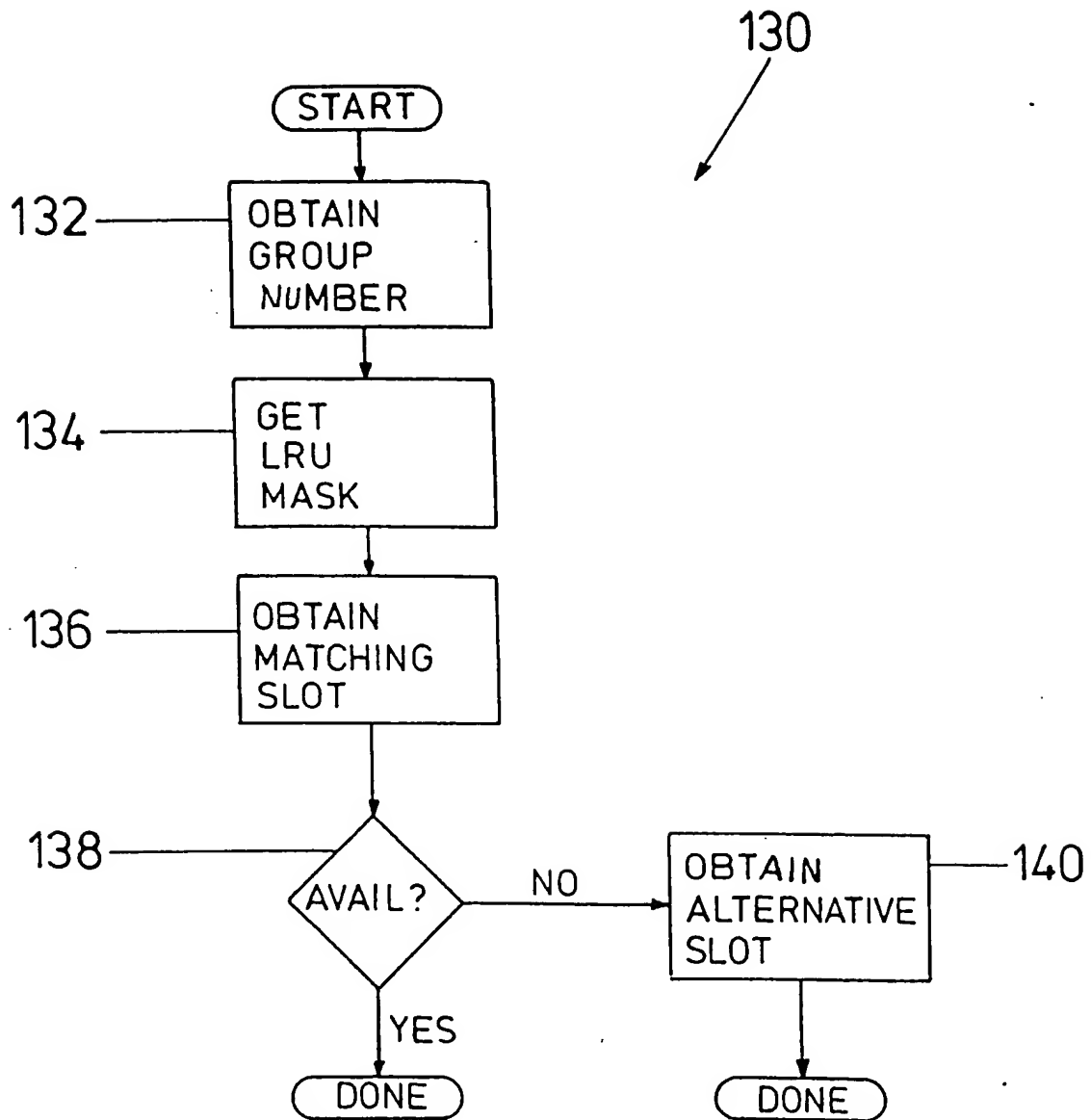


FIG 9

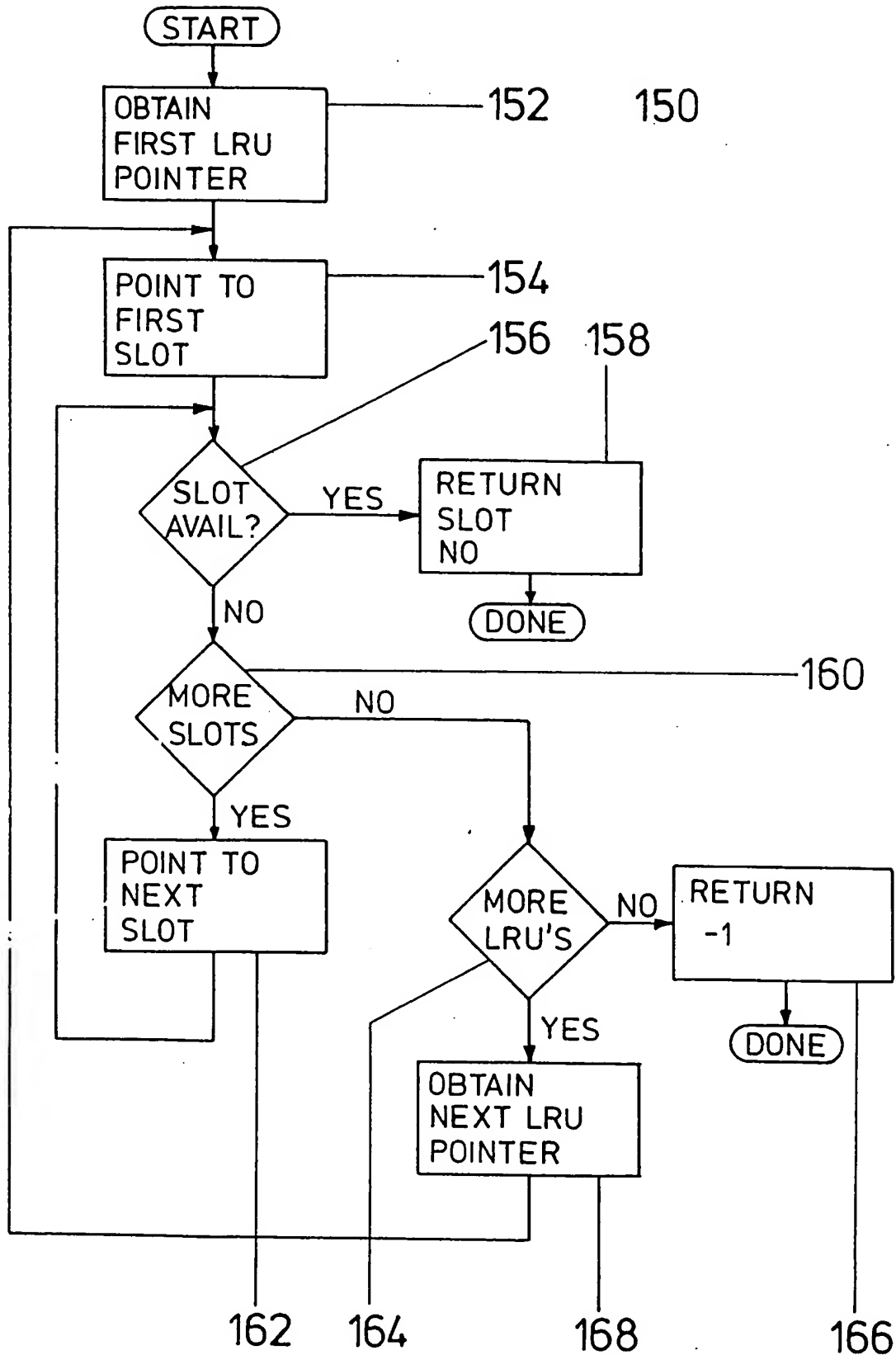




FIG 10

170

SLOT #	LRU
0	1
1	1
2	2
3	2
4	2
5	2
6	3
7	4
8	4
9	4
10	4
11	4
12	4